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Optimum multiplexer design in quantum-dot cellular automata

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is one of the most important computing technologies for the future and will be the alternative candidate for current CMOS technology. QCA is attracting a lot of researchers due to many features such as high speed, small size, and low power consumption. QCA has two main building blocks (majority gate and inverter) used for design any Boolean function. QCA also has an inherent capability that used to design many important gates such as XOR and Multiplexer in optimal form without following any Boolean function. This paper presents a novel design 2:1 QCA-Multiplexer in two forms. The proposed design is very simple, highly efficient and can be used to produce many logical functions. The proposed design output comes from the inherent capabilities of quantum technology. New 4:1 QCA-Multiplexer has been built using the proposed structure. The output waveforms showed the wonderful performance of the proposed design in terms of the number of cells, area, and latency.

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1. INTRODUCTION

In recent years, there have been many studies to replace CMOS technology that currently used in Integrated Circuits (ICs) with an alternative because of many reasons such as the power consumption and inability to continue following Moore's law [1], which states the number of transistors in a single chip. So, searching for alternatives became a priority for the researchers. QCA technology has many amazing features such as high speed, low complexity, and small size compared with traditional CMOS. Quantum cell is the basic building block in QCA circuits, each cell has four quantum dots injected with two electrons moving between those dots [2]. QCA uses the arrangement of intracellular electrons for binary representation instead of voltage level, so there is flow of current in this technique [3-5]. Many efforts have been made to implement the crucial components in logic circuits such as XOR [6-11] and multiplexer [12-18] using this nanotechnology. The multiplexer (MUX) was extensively utilized to implement many digital circuits such as RAM cells and ALU. The reliability of QCA circuit got the attention in [19]. This paper presents a novel structure 2:1 QCA-MUX. The proposed design has many enhancements in terms of area, latency, and complexity. The 4:1 multiplexer is carried out using the proposed structure.

Quantum cell is the brick in QCA circuits. Every cell, Square-formed, have four quantum dots. Two electrons are injected into each cell and these electrons have the ability to move between points so that they settle in a diagonal position because of the columbic repulsion dependence on driver cell [20]. Figure 1 illustrates cell polarization. Binary numbers 1 and 0 can be represented with the two polarizations of cell P = +1 and P= –1 respectively. QCA wire and logical functions can be implemented by forming a group of cells in an array.

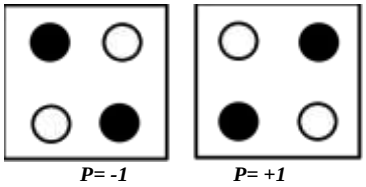

Figure 1. Cell Polarization

QCA wire is used to carry out the binary data transformation from the input cell to the output. Since the wire in the QCA consists of an array of cells, the binary data will be transferred to the output cell according to the principle of electronic repulsion [21]. The QCA wire is presented in two configurations; normal and rotated, as explained in Figure 2. To achieve coplanar wire crossing, the rotated wire is required or use another approach which introduced in [22] since there are other technique uses multi-layer but it is not promises for physical implementation.

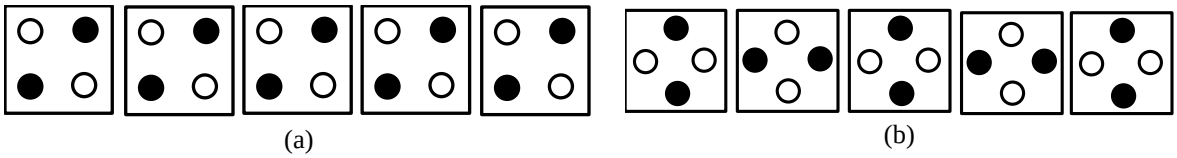

Figure 2. QCA wire (a) normal wire, (b) rotated wire

The main logic gates AND and OR can be performed utilizing the QCA universal gate (majority gate) by setting one of the inputs to 0 and 1 respectively. Majority gate is dominant in the QCA world with several studies focusing on it such as [23-27]. Two configurations of the majority gate are introduced in QCA as illustrated in Figure 3 [28]. The formula of the majority gate is given by 1.

$$M(A,B,C)=AB+BC+AC \quad (1)$$

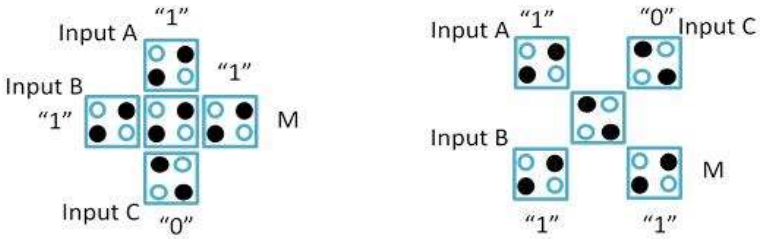

Figure 3. Majority gate forms

Generally, inverter with majority gate represents the fundamental blocks in QCA circuits, three forms of inverter were introduced in QCA as shown in Figure 4.

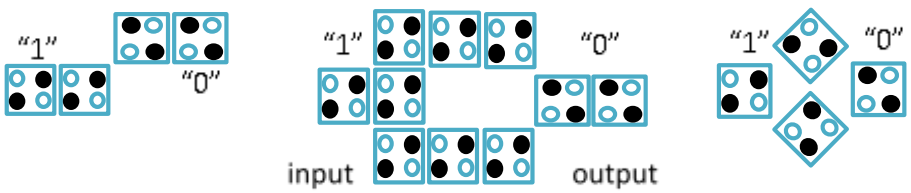

Figure 4. QCA inverter forms

To ensure data flow from input to output and to ensure cells synchronization, the clock is applied to all cells [20]. The barriers between the dots inside the cells are controlled by the clocking signal so that the cell is unpolarized as long as the clock is low. When the clock goes high, each cell gets polarized after the electrons move to the dots which need the lowest energy depending on the driver cell. Clock signal consists of four phases to guarantee adiabatic cell switching, (switch, hold, release and relax). QCA circuit can be divided into 4 zones where every zone comprises four phases as illustrated in Figure 5 [29].

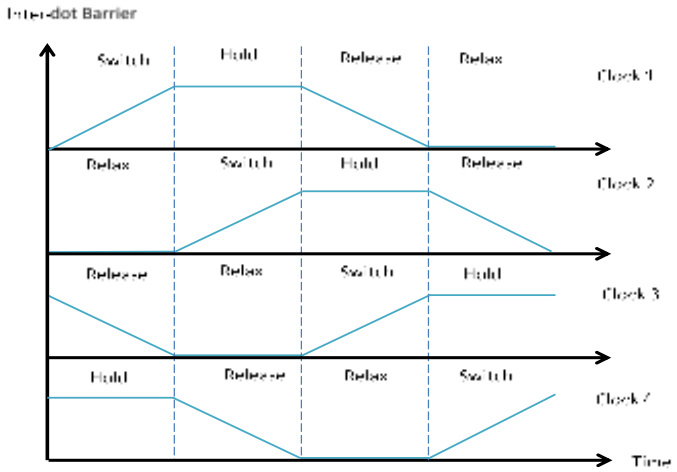

Figure 5. QCA Clock signal

Multiplexer circuit takes information from 2n lines where at each time one of the inputs send to the output depending on selector signals [13]. Table 1 shows the 2:1 multiplexer truth table. If S is 0 then the value of I0 goes to the output and if S is 1 then the value of I1 goes to the output. The output equation of multiplexer is given in 2. Figure 6. shows the previously proposed designs of 2:1 MUX. The first three structures consist of 2-input AND gates, 2-input OR gate and inverter as the schematic diagram is shown in Figure 7. [3] while the last structure uses the inherent capabilities of QCA to get the output. The design in Figure 6 (a) uses 0.03 µm2 and consists of 27 cells with 3 clock zone latency. The design in Figure 6 (b) uses 0.02 µm2 and consists of 26 cells with 2 clock zone latency. The design in Figure 6 (c) uses 0.02 µm2 and consists of 23 cells with 2 clock zone latency. While the design in Figure 6 (d) uses 0.01 µm2 and consists of 12 cells with 1 clock zone latency.

$$Out = S.I_1 + \overline{S}.I_0 \quad (2)$$

Table 1. 2:1 Mux Truth Table

S	Out
0	I_0
1	I_1

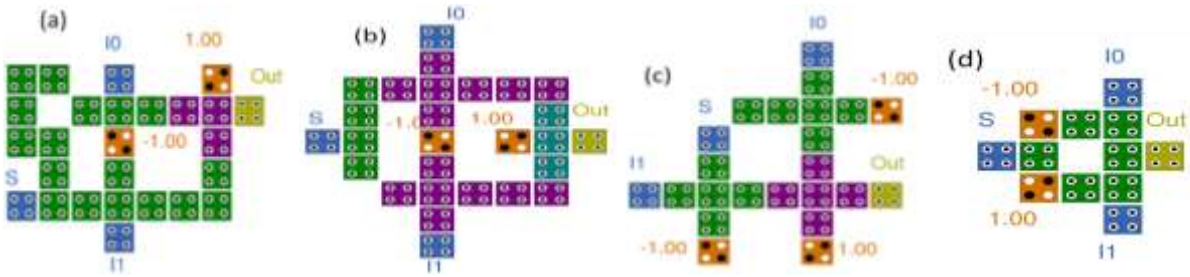

Figure 6. 2:1 MUX presented (a) in [30], (b) in[31], (c) in[32]and (d) in [13]

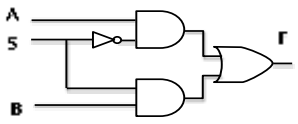

Figure 7. Logic circuit diagram of 2:1 Multiplexer

1.1. The Proposed Circuits

This section divided into two parts, the first part presents tow new structures of 2:1 Multiplexer, that can be interchanged depending on the circuit requirements, and in the second part new 4:1 multiplexer is implemented using the unique structure which was proposed in the first part.

1.2. Proposed 2:1 Multiplexer

The schematic of the multiplexer and the layouts of the proposed two circuits are shown in Figure 8. (a), (b) and (c) respectively. It contains two inputs (I0, I1), one output (Out) and one selector (S).

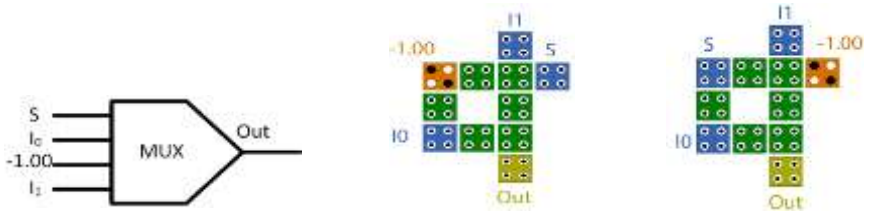

Figure 1. Proposed 2:1 QCA-MUX (a) Schematic, (b) Layout 1, (c) Layout 2

1.3. Proposed 4:1 Multiplexer

The 4:1 MUX contains 4 inputs (I_0, I_1, I_2, and I_3), 1 output (Out) and 2 selectors (S_0S_1). The truth table of this Multiplexer is illustrated in Table 2. The Out equal to I_0 when S_0S_1=00, when S_0S_1=01 the Out =I_1 however, the Out equal to I_2 and I_3 if S_0S_1 equal to 10 and 11 respectively. The 4:1 Multiplexer constructed of three 2:1 multiplexer and the formula of this multiplexer is given in 3. Figure 9 shows the schematic and structure layout of the proposed 4:1 multiplexer.

Table 2. 4:1 QCA-Mux Truth Table

S_0S_1	Out
00	I_0
01	I_1
10	I_2
11	I3

$$\text{Out} = (\overline{S_0}\,\overline{S_1})I_0 + (\overline{S_0}S_1)I1 + (S_0\overline{S_1})I2 + (S_0S_1)I3 \quad (3)$$

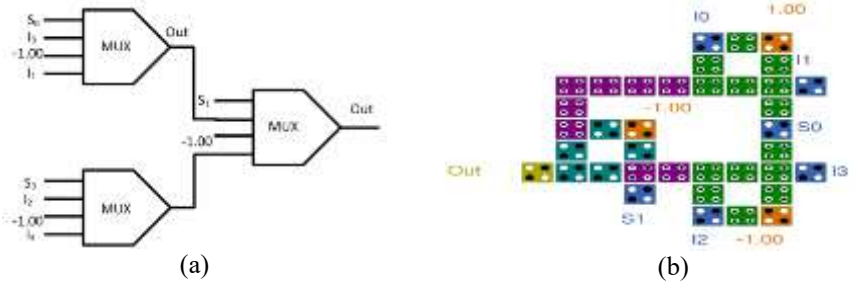

Figure 9. Proposed 4:1 MUX (a) Schematic, (b) Layout

2. METHODOLOGY

The Proposed multiplexers are verified by QCADesigner V 2.0.3, with the default simulation parameters. Figure 10 shows the simulation result of the proposed 2:1 QCA-MUX. The output waveforms proved that they were identical to what is expected without delay because input and output are in the same clock zone. The proposed unique 2:1 multiplexer uses 0.01 μm^2 and consists of 11 cells with 1 clock zone latency. The result of the simulation for the second proposed structure, 4:1 multiplexer, is illustrated in Figure 11. This QCA circuit consists of 37 cells with 0.03 μm^2 and 3 clock zone latency. This result is extremely distinguished in QCA multiplexer designs.

Figure 10. Output waveforms for the proposed 2:1 MUX

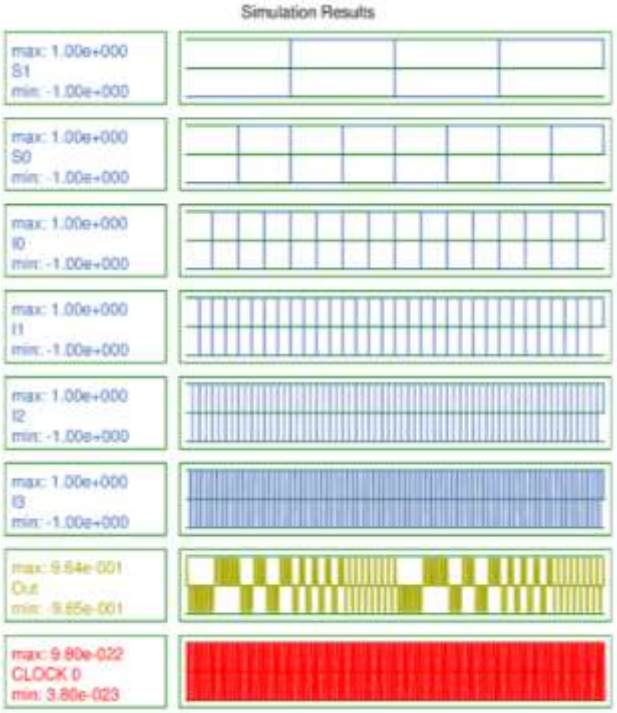

Figure 11. Output waveforms for the proposed 4:1 MUX

3. RESULTS AND DISCUSSION

This section shows the performance of the proposed circuits by comparing the result with previous designs. Table 3 illustrate the comparison result for the first MUX, 2:1 multiplexer, proposed with existing counterparts. While the comparison results of the second proposed gate, 4:1 multiplexer, is shown in Table 4.

Table 3. Comparative Result of 2:1 Multiplexer

2:1 Mux	Area (μm^2)	No. of Cells	Crossover type	Latency (Clock zone)
[33]Fig. 9	0.28	146	Multilayer	8
[33]Fig. 8	0.14	88	Multilayer	4
[34]	0.14	67	Coplanar	4
[35]	0.07	56	Coplanar	4
[36]	0.08	46	Coplanar	4
[15]	0.06	36	Multilayer	4
[37]	0.04	35	Coplanar	4
[38]	0.03	27	Coplanar	3
[31]	0.02	26	Coplanar	2
[32]	0.02	23	Coplanar	2
[16]	0.02	19	Coplanar	2
[39]	0.02	19	Coplanar	3
[3]	0.01	15	Coplanar	2
[13]	0.01	12	Without	1
proposed	0.01	11	Without	1

Table 4. Comparative Result of 4:1 Multiplexer

4:1 Mux	Area (μm^2)	No. of Cells	Crossover type	Latency (Clock zone)
[35]	0.35	290	Coplanar	6
[31]	0.37	271	Coplanar	19
[40]	0.2	251	Multilayer	5
[41]	0.22	223	Multilayer	6
[34]	0.25	215	Coplanar	6
[40]	0.27	199	Coplanar	6
[32]	0.24	155	Coplanar	5
[37]	0.25	124	Coplanar	8
[3]	0.15	107	Coplanar	4
[13]	0.08	61	Coplanar	4
Proposed	0.03	37	Without	3

The power dissipation of the above circuits including the two layouts of the proposed multiplexer can be estimated using QCAPro tool. This tool capable of dealing with a large number of cells because it utilizes a fast approximation-based technique and it can expect non-adiabatic switching power losses with polarization error in QCA circuit. In this work, the value of temperature 2k has been taken in QCAPro parameter. The comparative analysis of dissipated power at different levels of tunneling energy (0.5Ek, 1Ek, and 1.5Ek) for 2:1 Multiplexer are shown in Table 5. The maps of dissipated power for the presented circuits with (0.5Ek) tunneling energy are illustrated in Figure 12.

Table 5. Power Analysis Result

Circuit	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Total energy consumption (meV)		
	0.5Ek	1Ek	1.5Ek	0.5Ek	1Ek	1.5Ek	0.5Ek	1Ek	1.5Ek
In [30]	7.36	21.78	38.79	32.40	28.23	24.20	39.76	50.01	62.99
In [31]	8.19	23.80	41.82	29.15	25.06	21.21	37.34	48.86	63.03
In [32]	7.23	20.54	35.68	24.37	20.77	17.48	31.60	41.31	53.16
In [13]	3.43	9.61	16.46	11.54	9.50	7.86	14.97	19.11	24.32
Proposed1	2.66	7.72	13.59	11.15	9.90	8.63	13.81	17.62	22.22
Proposed2	2.54	7.50	13.35	8.07	7.04	6.07	10.61	14.54	19.42

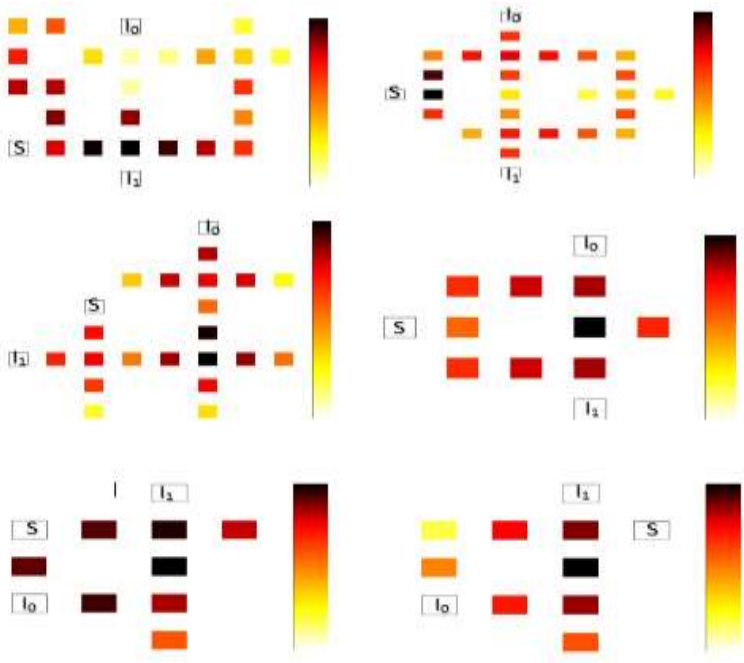

Figure 12. Dissipated power maps for multiplexer presented (a) in [30], (b) in[31], (c) in[32], (d) in [13], (e) proposed layout 1, (f) proposed layout 2

4. CONCLUSION

This paper proposes a novel highly efficient two forms singular 2:1 QCA-MUX circuit simulated by QCADesigner tool. The proposed gate does not follow any logical functions. It is derived from the inherent capabilities of quantum technology to give the correct output. A new structure of 4:1 multiplexer has been designed with coherence vector engine using the proposed 2:1 multiplexer. The unique feature for the 4:1 multiplexer is that it was done without any crossover. The proposed designs prove that it has less complexity as well as being cost effective compared to the typical multiplexers. The simulation results obtained from the QCADesigner tool show that the structures presented in this work show an improvement in terms of area, delay and cell count putting in mind that all inputs and outputs are in the circuit terminals which gives real single layer design without wire crossing.

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